How to Grade Layouts

# JLCPCB

Upload the zipped Gerber files to the [JLCPCB instant quote.](https://cart.jlcpcb.com/quote?orderType=1&stencilLayer=2&stencilWidth=100&stencilLength=100&stencilCounts=5)

Check for first immediate issues that can be caught and that the board is showing up as you would expect it to-

* Silk Screen issues
  + Missing or incorrectly placed reference designators (e.g., overlapping pads or holes)
  + Missing or incorrectly placed names
* No traces or pads being cut off by the edge

# Gerber Viewer

To check all the specific details of the board, go to the C drive and open the folder *GerberViewer* and click on “gerbv”. Go to *File* > *Open Layer(s)* or press Ctrl + O. Navigate to the unzipped Gerber files of the project and open all 8 files: *Board\_Outline.GKO, Bottom\_Layer.GBL, Bottom\_Silkscreen.GBO, Bottom\_Soldermask.GBS, ThruHolePlated.ncd, Top\_layer.GTL, Top\_Silkscreen.GTO, Top\_Soldermask.GTS.*

*(****Note:*** *The NC Drill file (.ncd) is required to be in the same folder as the other Gerber files)*

You can use the zoom tool (*Tools > Zoom Tool*) to help zoom in right on your board.

Deselect all layers and view each one individually in relation to the other layers.

1. Board Outline
   1. Leave this on as you inspect all other layers and ensure that none of them are outside of this outline.
2. Bottom
   1. Check that the Bottom Soldermask shows up and is over the Bottom Layer header pins
   2. Check that any text on the bottom silkscreen is showing up backwards on the Gerber Viewer (they will show up normal on JLCPCB).
   3. If there are vias these should show up on the bottom layer as well.
   4. There should be no pads on the bottom layer.
3. NC Drill File
   1. Keeping the bottom layer on turn on the NC Drill hole layer. Holes should show up in the center of all header pins and via holes.
   2. If holes are not showing up, right click on the drill file and select *Edit File Format*. Deselct autodetect and try out different integers in the digits box until your drill holes line up in the center of your header pins and via holes.
4. Size Constraints
   1. Keeping only the board outline and the NC Drill file selected turn on the Top Layer, again ensuring that Drill Holes are still lined up properly.
   2. Using the Measure Tool (*Tools > Measure Tool*) measure the different constraints on the board according to the Lab document. Measure from the center of the (bottom left) drill hole to the edge of the board outline, see below.

A picture containing graphical user interface

Description automatically generated

* 1. The measurements can be less than or equal to constraints given to ensure that the daughter PCB will fix in the chassis. However, designing the smallest PCB possible should be the goal. Thus, look for ways to conserve space and decrease the size of the board outline if possible.

1. Top Layer
   1. On the Top Layer measure the traces to ensure they are 10 th.
   2. During the third and fifth labs ensure that pads are correctly sized. (The third lab is the first time using the resistor pads and the fifth is the first time using the capacitor pads from the myCentralLibrary made in Lab 1).
   3. Check that there are traces connected to each component on the board. If there are any components that do not have a trace connected to them, then there is something wrong. Sometimes traces are connected to the header pins from the bottom layer. (**Note:** Lab 5 if you use a ground plane there will be no traces connected to the ground header pin but it should be connected to the plane.)
2. Top
   1. View the Top Solder Mask and ensure that it is covering all pads and header pins from the top layer.
   2. Leave only the top solder mask and the board outline on, then turn on the Top Silkscreen. Ensure that there is nothing from the silkscreen (reference designators or names) overlapping and getting cut off by pads or header pins.

# Tips for Resubmissions

When editing your board to resolve any issues, be sure to keep a couple of things in mind-

* If you change the position of reference designators, you need to regenerate the silkscreen. Upload to JLCPCB or open in gerbv.exe to make sure any changes you make are reflected there.
* If you change the position of your vias or header pins, then you need to generate a new NC Drill File. If you do not, your drill holes will be in the wrong position.
* If you change the trace widths in your constraint manager, then you will still need to change the trace widths of the traces you have already placed. Under Loc: Routing you can select the whole board, right-click, and update most of the trace widths there. It will **not** update ones that are in positions where they will no longer fit if they were updated.